TED (15) – 3131

(REVISION — 2015)

Reg. No.....

Signature .....

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE — OCTOBER, 2018

COMPUTER ARCHITECTURE (CT)

[*Time* : 3 hours

(Maximum marks : 100)

PART — A

(Maximum marks : 10)

Marks

I Answer *all* questions in one or two sentences. Each question carries 2 marks.

1. Define PC.
2. What are the various methods of bus arbitration ?
3. Define CAV.
4. Mention any two categories of user-visible registers.
5. Define SIMD.

(5×2 = 10)

PART — B

(Maximum marks : 30)

II Answer any *five* of the following questions. Each question carries 6 marks.

1. Draw and explain a typical memory hierarchy.
2. Draw the memory cell structures of static RAM and Dynamic RAM.
3. Explain the block format of a CD-ROM.
4. Draw the internal Structure of CPU.
5. Draw and explain the micro-architecture of the control unit.
6. Explain different types of data hazards.
7. Explain different I/O commands that an I/O module receive when it is addressed by a processor.

(5×6 = 30)

[P.T.O.

Marks

PART — C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks.)

UNIT — I

III (a) List and explain two approaches to dealing with multiple Interrupts. 6

(b) Draw the timing diagrams of synchronous bus operations and asynchronous bus operations. 9

OR

IV (a) List and explain the characteristics of computer memory system. 10

(b) Draw the structure of single cache organization and three level cache organization. 5

UNIT — II

V Explain data organization and formatting mechanism in magnetic data. 15

OR

VI (a) Compare RAID levels. 9

(b) What are major functions of I/O module. 6

UNIT — III

VII (a) A pipelined processor has a clock rate of 5GHz and execute a program with 10 instructions. The pipeline has 5 stages and instructions are issued at a rate of one per clock cycle. Ignore penalties due to branch instruction and out of sequence execution. What is the speed up of this processor for this program compared to a non-pipelined processor ? 9

(b) If the last operation performed on a computer with 8-bit word was an addition in which two operands are 00001100 and 01001010. What would be the value of Carry, Zero, Overflow, Even parity, Half Carry, Sign flags after the operation ? 6

OR

VIII (a) With a neat sketch explain about instruction cycle state diagram. 12

(b) Explain about resource hazards. 3

UNIT — IV

IX (a) Explain symbolically the different sequence of events occur during Fetch, Indirect, Interrupt, Execute Cycle. 12

(b) Outline a three step process leads to the characterization of control unit. 3

OR

X (a) Draw and explain the architecture of cpu with internal bus. 7

(b) List and explain Flynn's classification of parallel processing system. 8

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