TED (15/19) -3042
(Revision -2015/19)

A22-08284

Reg.No…….....
Signature. .....

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/
COMMERCIAL PRACTICE – APRIL -2022.

DIGITAL ELECTRONICS

(Maximum Marks : 100) [Time : 3 hours]

PART–A

(Maximum marks: 10) Marks

I. Answer **all** questions in one or two sentences. Each question carries 2 marks.

1. Define radix of a number.
2. Draw symbols of universal gates.
3. Define fan-in.
4. Write any two applications of shift register.
5. List different types of ADCs. (5x2=10)

PART - B

(Maximum Marks : 30)

II Answer any **five** of the following questions . Each question carries 6 marks.

1. Convert the following binary numbers to decimal (a)1011 (b)1101101
   (c)1101110.011.
2. Implement all logic gates using NAND gate only.
3. Draw and explain the working principle of TTL inverter.
4. Implement the Full adder circuit using NAND gates only.
5. Draw and explain J-K Flip flop using NAND gates.
6. Explain the working principle of Johnson-counter.
7. With a neat sketch explain the working principle of MOD-10 asynchronous counter using J-K flip-flop. (5x6 =30)

PART - C

(Maximum marks : 60)

(Answer one full question from each unit. Each full question carries 15 marks)

UNIT I

III (a) Perform the following binary operations

(i)11011+1101 (ii) 10111.101+110111.01 (3)1110-1001 (iv)1101-1010 (8)

(b) State Demorgans Theorem … Reduce the following expression using K-map

F= $\sum$ m(5,6,7,9,10,11,13,14,15) (7)

OR

IV (a) Explain the operation of AND,NAND and EXOR gates with their symbols and truth tables. (9)

(b) Reduce the following Boolean expressions.

(i)A($\bar{A}$ +BC) (ii) A(BC+$\bar{B}$C) (iii)AAB($\bar{A}$BC + BBC) (6)

UNIT- II

V (a) Compare TTL and ECL logic families. (8)

(b) Draw and Explain the working principle of 4X1 multiplexer. (7)

OR

VI (a) Explain the working principle of CMOS NAND gate. (8)

(b) Draw the circuit of Binary-to-gray code converter and explain. (7)

UNIT- III

VII (a) Compare D and T Flip-flops. (8)

(b) State race around condition in J-K Flip-flop and list the methods for eliminating race around condition. (7)

OR

VIII (a) Draw and explain the working principle of serial in serial out shift register. (8)

(b) Describe the working principle of ring counter. (7)

UNIT – IV

IX (a) Draw and explain the working principle of 3 bit up-down counter J-K flip-flop. (9)

(b) Differentiate between synchronous and asynchronous counters. (6)

OR

X (a) Explain R-2R Ladder type digital to analog converter with a diagram. (8)

(b) Describe Flash type ADC. (7)

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